

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



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MA	4,928,265	05/22/90	Higuchi et al.	—	—	
MA	4,953,130	08/28/90	Houston	—	—	
MA	5,251,309	10/05/93	Kinoshita et al.	—	—	
MA	4,099,231	07/01/78	Kotok et al.	—	—	

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MA	JP-A-1-236494	09/21/89	JP	-	-	YES
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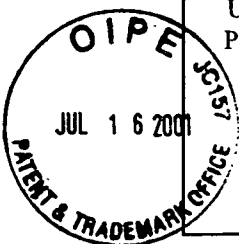
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<i>MA</i>	Sho 60-80193	May 8, 1983	Japan	—	—	YES
<i>MA</i>	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES
<i>MA</i>	S61-72350	April 14, 1986	Japan	—	—	YES
<i>MA</i>	S63-142445	June 14, 1988	Japan	—	—	YES
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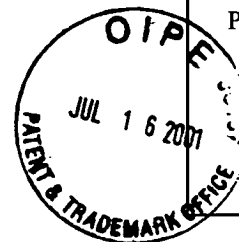
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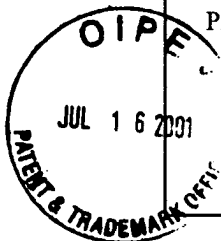
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<i>GA</i>	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
<i>GA</i>	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
<i>GA</i>	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
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	APPLICANT(S) FARMWALD ET AL.	
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MA	4,975,872	12/04/90	Zaiki	—	—	
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BA	4,860,198	08/22/89	Takenaka	—	—	
MA	3,969,706	07/13/76	Proebsting et al.	—	—	
DA	4,766,536	08/23/88	Wilson, Jr. et al.	—	—	
MA	4,998,262	03/05/91	Wiggers	—	—	
DA	4,757,473	07/12/88	Kurihara et al.	—	—	
MA	4,792,926	12/20/88	Roberts	—	—	
DA	4,811,202	03/07/89	Schabowski	—	—	
DA	5,034,917	07/23/91	Bland et al.	—	—	
MA	5,301,278	04/05/94	Bowater et al.	—	—	
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BA	4,509,142	04/02/85	Childers	—	—	
MA	5,051,889	09/24/91	Fung et al.	—	—	
MA	5,361,277	11/01/94	Grover	—	—	
BA	4,954,987	09/04/90	Auvinen et al.	—	—	
BA	4,570,220	02/11/86	Tetrick et al.	—	—	
BA	4,247,817	01/27/81	Heller	—	—	
BA	4,519,034	05/21/85	Smith et al.	—	—	
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<i>MA</i>	5,023,488	06/11/91	Gunning	—	—	
<i>MA</i>	4,754,433	06/28/88	Chin et al.	—	—	
<i>MA</i>	3,771,145	11/06/73	Wiener	—	—	
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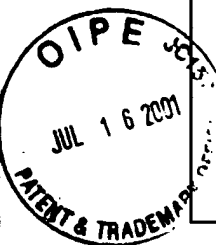
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MA	4,916,670	04/10/90	Suzuki et al.	—	—	
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MA	Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985)
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MA	Dave Bursky, "ADVANCED SELF-TIMED SRAM PARES ACCESS TIME TO 5 NS", Electronic Design, pp. 145-147 (Feb. 22, 1990)

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MA	SHO 58-192154	Nov. 9, 1983	Japan	—	—	NO	
MA	SHO 63-34795	Feb. 15, 1988	Japan	—	—	NO	
MA	SHO 61-107453	May 26, 1986	Japan	—	—	NO	
MA	SHO 63-91766	April 22, 1988	Japan	—	—	YES	
MA	SHO 62-16289	Jan. 24, 1987	Japan	—	—	NO	
MA	SHO 61-160556	Oct. 4, 1986	Japan	—	—	NO	

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MA	5,029,124	07/02/91	Leahy et al.	—	—	
MA	5,193,193	03/09/93	Iyer	—	—	
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MA	4,566,099	01/21/86	Magerl	—	—	
MA	4,803,621	02/07/89	Kelly	—	—	
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MA	4,761,567	Aug. 2, 1988	Walters, Jr. et al.	307	269	
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MA	sho 60-261095A	June 6, 1984	Japan	/	/	
MA	sho 63-300310	Dec. 7, 1988	Japan	/	/	
MA	hei 2-8950	Jan 12, 1990	Japan	/	/	
MA	sho 58-184626A	Oct 28, 1983	Japan	/	/	

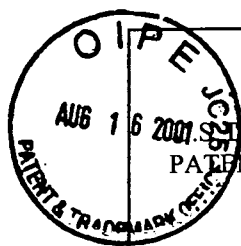
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MA	"ECL bus controller hits 266 Mbytes/s" Microprocessor Report, MicroDesign Resources Inc., Vol. 4: No. 1; Pg. 12, Jan. 24, 1990

EXAMINER <i>Gilma Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	